

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	462	(ris\$3 near2 transition\$1 or lead\$3 near2 transition or rais\$3 near2 transition\$1 or lag\$4 near2 transition\$1 or fall\$3 near2 transition\$1 or fail\$4 near2 transiton\$1) near5 (greater or bigger or smaller or longer or taller or higher or lower)	US- PGPUB ; USPAT ; EPO; JPO	2006/08/1 6 14:33	
2	BRS	L2	25	(combin\$3 near2 delay\$3 or add\$3 near3 delay\$3 or sum\$4 near3 delay\$3 or subtract\$3 near3 delay\$3) and 1	US- PGPUB ; USPAT ; EPO; JPO	2006/08/1 6 14:31	
3	BRS	L3	14	(ris\$3 near2 transition\$1 or lead\$3 near2 transition or rais\$3 near2 transition\$1 or lag\$4 near2 transition\$1 or fall\$3 near2 transition\$1 or fail\$4 near2 transiton\$1) near5 (greater or bigger or smaller or longer or taller or higher or lower) with (input) with (output)	US- PGPUB ; USPAT ; EPO; JPO	2006/08/1 6 14:26	
4	BRS	L4	12	3 not 2	US- PGPUB ; USPAT ; EPO; JPO	2006/08/1 6 14:30	

	Error Definition	Err ors
1		
2		
3		
4		

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L5	86	((WILLIAM) near2 (DALLY)).INV.	US- PGPUB ; USPAT ; USOCR	2006/08/1 6 14:29	
6	BRS	L6	33	((JOHN) near2 (POULTON)).INV.	US- PGPUB ; USPAT ; USOCR	2006/08/1 6 14:30	
7	BRS	L7	95	5 or 6	US- PGPUB ; USPAT ; EPO; JPO	2006/08/1 6 14:31	
8	BRS	L8	0	1 and 7	US- PGPUB ; USPAT ; EPO; JPO	2006/08/1 6 14:31	
9	BRS	L9	15	(combin\$3 near2 delay\$3 or add\$3 near3 delay\$3 or sum\$4 near3 delay\$3 or subtract\$3 near3 delay\$3) and 7	US- PGPUB ; USPAT ; EPO; JPO	2006/08/1 6 14:31	
10	BRS	L10	1	(ris\$3 near2 transition\$1 or lead\$3 near2 transition or rais\$3 near2 transition\$1 or lag\$4 near2 transition\$1 or fall\$3 near2 transition\$1 or fail\$4 near2 transiton\$1)and 7	US- PGPUB ; USPAT ; EPO; JPO	2006/08/1 6 14:33	

	Error Definition	Err ors
5		
6		
7		
8		
9		
10		

Day : Wednesday

Date: 8/16/2006

Time: 14:34:03



PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = DALLY

First Name = WILLIAM

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60237086	Not Issued	159	09/28/2000	Multistage digital cross connect with synchronized configuration switching and integral frame timing	DALLY, WILLIAM J.
60248273	Not Issued	159	11/14/2000	Scheduling clos networks	DALLY, WILLIAM J.
09140030	6430527	150	08/26/1998	PREFIX SEARCH CIRCUITRY AND METHOD	DALLY, WILLIAM J.
09498413	6728240	150	02/04/2000	SERIAL LINK CIRCUIT INCLUDING CAPACITIVE OFFSET ADJUSTMENT OF A HIGH-SPEED RECEIVER	DALLY, WILLIAM J.
09557164	Not Issued	80	04/25/2000	Transition-time control in a high-speed data transmitter	DALLY, WILLIAM J.
09557564	6674772	150	04/25/2000	DATA COMMUNICATIONS CIRCUIT WITH MULTI-STAGE MULTIPLEXING	DALLY, WILLIAM J.
09557640	6952431	150	04/25/2000	CLOCK MULTIPLYING DELAY-LOCKED LOOP FOR DATA COMMUNICATIONS	DALLY, WILLIAM J.
09588619	6891834	150	06/06/2000	APPARATUS AND METHOD FOR PACKET SCHEDULING	DALLY, WILLIAM J.
09591510	Not Issued	93	06/12/2000	Data transfer bus communication using single request to perform command and return data to destination indicated in context to allow thread context switch	DALLY, WILLIAM J.
09625650	6426656	150	07/26/2000	HIGH SPEED, LOW-POWER INTER-CHIP TRANSMISSION SYSTEM	DALLY, WILLIAM J.
09625802	6965299	150	07/26/2000	HIGH-SPEED, LOW-POWER CROSSBAR SWITCH	DALLY, WILLIAM J.
09757740	Not	160	01/09/2001	Flit-reservation flow control	DALLY, WILLIAM

	Issued				J.
<u>09758402</u>	Not Issued	161	01/09/2001	Flit-reservation flow control	DALLY, WILLIAM J.
<u>09761172</u>	6870838	150	01/16/2001	MULTISTAGE DIGITAL CROSS CONNECT WITH INTEGRAL FRAME TIMING	DALLY, WILLIAM J.
<u>09761538</u>	Not Issued	41	01/16/2001	Multistage digital cross connect with synchronized configuration switching	DALLY, WILLIAM J.
<u>09761539</u>	Not Issued	41	01/16/2001	Time slot interchanger	DALLY, WILLIAM J.
<u>09765138</u>	6606656	150	01/18/2001	APPARATUS AND METHODS FOR CONNECTING MODULES USING REMOTE SWITCHING	DALLY, WILLIAM J.
<u>09849920</u>	6937073	150	05/04/2001	FREQUENCY MULTIPLIER WITH PHASE COMPARATOR	DALLY, WILLIAM J.
<u>09852481</u>	6542555	150	05/10/2001	DIGITAL TRANSMITTER WITH EQUALIZATION	DALLY, WILLIAM J.
<u>09871301</u>	7100026	150	05/30/2001	SYSTEM AND METHOD FOR PERFORMING EFFICIENT CONDITIONAL VECTOR OPERATIONS FOR DATA PARALLEL ARCHITECTURES INVOLVING BOTH INPUT AND CONDITIONAL VECTOR VALUES	DALLY, WILLIAM J.
<u>09887960</u>	6654381	150	06/22/2001	METHODS AND APPARATUS FOR EVENT-DRIVEN ROUTING	DALLY, WILLIAM J.
<u>09891233</u>	6617936	150	06/22/2001	PHASE CONTROLLED OSCILLATOR	DALLY, WILLIAM J.
<u>09925753</u>	6476656	150	08/09/2001	LOW-POWER LOW-JITTER VARIABLE DELAY TIMING CIRCUIT	DALLY, WILLIAM J.
<u>09992528</u>	Not Issued	160	11/14/2001	Scheduling clos networks	DALLY, WILLIAM J.
<u>10017362</u>	Not Issued	161	12/14/2001	Internet switch router	DALLY, WILLIAM J.
<u>10021205</u>	Not Issued	41	12/07/2001	Composite trunking	DALLY, WILLIAM J.
<u>10052233</u>	6807186	150	01/17/2002	ARCHITECTURES FOR A SINGLE-STAGE GROOMING SWITCH	DALLY, WILLIAM J.
<u>10141499</u>	Not Issued	40	05/07/2002	Scheduling clos networks	DALLY, WILLIAM J.

<u>10167689</u>	Not Issued	161	06/11/2002	Prefix search circuitry and method	DALLY, WILLIAM J.
<u>10172535</u>	6614268	150	06/13/2002	HIGH-SPEED, LOW- POWER INTER-CHIP TRANSMISSION SYSTEM	DALLY, WILLIAM J.
<u>10178902</u>	Not Issued	71	06/21/2002	Digital clock recovery circuit	DALLY, WILLIAM J.
<u>10246805</u>	Not Issued	71	09/18/2002	Internet switch router	DALLY, WILLIAM J.
<u>10325700</u>	Not Issued	30	12/18/2002	Method and system for guaranteeing quality of service in large capacity input output buffered cell switch based on minimum bandwidth guarantees and weighted fair share of unused bandwidth	DALLY, WILLIAM J.
<u>10325701</u>	Not Issued	30	12/18/2002	Method and apparatus for ensuring cell ordering in large capacity switching systems and for synchronizing the arrival time of cells to a switch fabric	DALLY, WILLIAM J.
<u>10339796</u>	Not Issued	30	01/09/2003	Weighted fair share scheduler for large input-buffered high-speed cross-point packet/cell switches	DALLY, WILLIAM J.
<u>10372630</u>	7099404	150	02/24/2003	DIGITAL TRANSMITTER	DALLY, WILLIAM J.
<u>10456121</u>	6976064	150	06/06/2003	APPARATUS AND METHODS FOR CONNECTING MODULES USING REMOTE SWITCHING	DALLY, WILLIAM J.
<u>10457718</u>	7043562	150	06/09/2003	IRREGULAR NETWORK	DALLY, WILLIAM J.
<u>10615819</u>	6861916	150	07/09/2003	PHASE CONTROLLED OSCILLATOR	DALLY, WILLIAM J.
<u>10628312</u>	Not Issued	93	07/28/2003	PREFIX SEARCH METHOD	DALLY, WILLIAM J.
<u>10673912</u>	Not Issued	30	09/29/2003	Methods and apparatus for event-driven routing	DALLY, WILLIAM J.
<u>10695069</u>	Not Issued	30	10/28/2003	Data communications circuit with multi-stage multiplexing	DALLY, WILLIAM J.
<u>10775594</u>	Not Issued	30	02/10/2004	Space-efficient source routing	DALLY, WILLIAM J.
<u>10815458</u>	Not Issued	30	04/01/2004	Adaptive source routing and packet processing	DALLY, WILLIAM J.
<u>10926122</u>	Not Issued	30	08/25/2004	Fabric router with flit caching	DALLY, WILLIAM J.

10944616	Not Issued	30	09/17/2004	Method and apparatus for data recovery	DALLY, WILLIAM J.
11019979	7047391	150	12/21/2004	SYSTEM AND METHOD FOR RE-ORDERING MEMORY REFERENCES FOR ACCESS TO MEMORY	DALLY, WILLIAM J.
11040628	7088270	150	01/21/2005	A LOW POWER, DC-BALANCED SERIAL LINK	DALLY, WILLIAM J.
11040835	7061406	150	01/21/2005	LOW POWER, DC-BALANCED SERIAL LINK TRANSMITTER	DALLY, WILLIAM J.
11040845	Not Issued	41	01/21/2005	Communication system with low power, DC-balanced serial link	DALLY, WILLIAM J.

[Search and Display More Records.](#)

Search Another: Inventor	Last Name	First Name	<input type="button" value="Search"/>
	<input type="text" value="DALLY"/>	<input type="text" value="WILLIAM"/>	

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)

Day : Wednesday

Date: 8/16/2006

Time: 14:34:13


PALM INTRANET
Inventor Name Search Result

Your Search was:

Last Name = POULTON

First Name = JOHN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60611039	Not Issued	159	09/17/2004	Bicycle drive	POULTON, JOHN F.
60160950	Not Issued	159	10/22/1999	LOW-POWER LOW-JITTER VARIABLE DELAY ELEMENTS	POULTON, JOHN W.
09557164	Not Issued	80	04/25/2000	Transition-time control in a high-speed data transmitter	POULTON, JOHN W.
09557564	6674772	150	04/25/2000	DATA COMMUNICATIONS CIRCUIT WITH MULTI-STAGE MULTIPLEXING	POULTON, JOHN W.
09557640	6952431	150	04/25/2000	CLOCK MULTIPLYING DELAY-LOCKED LOOP FOR DATA COMMUNICATIONS	POULTON, JOHN W.
09849920	6937073	150	05/04/2001	FREQUENCY MULTIPLIER WITH PHASE COMPARATOR	POULTON, JOHN W.
09891233	6617936	150	06/22/2001	PHASE CONTROLLED OSCILLATOR	POULTON, JOHN W.
09925753	6476656	150	08/09/2001	LOW-POWER LOW-JITTER VARIABLE DELAY TIMING CIRCUIT	POULTON, JOHN W.
10052233	6807186	150	01/17/2002	ARCHITECTURES FOR A SINGLE-STAGE GROOMING SWITCH	POULTON, JOHN W.
10615819	6861916	150	07/09/2003	PHASE CONTROLLED OSCILLATOR	POULTON, JOHN W.
10695069	Not Issued	30	10/28/2003	Data communications circuit with multi-stage multiplexing	POULTON, JOHN W.
11001865	Not Issued	71	12/01/2004	Wide-range multi-phase clock generator	POULTON, JOHN W.
11004343	Not Issued	71	12/03/2004	Adaptive bias scheme for high-voltage compliance in serial links	POULTON, JOHN W.
11015200	Not	30	12/17/2004	Low-capacitance electro-static	POULTON, JOHN

	Issued			discharge protection	W.
<u>11016234</u>	Not Issued	30	12/17/2004	Diode with reduced forward-bias resistance and shunt capacitance	POULTON, JOHN W.
<u>11040628</u>	7088270	150	01/21/2005	A LOW POWER, DC-BALANCED SERIAL LINK	POULTON, JOHN W.
<u>11040835</u>	7061406	150	01/21/2005	LOW POWER, DC-BALANCED SERIAL LINK TRANSMITTER	POULTON, JOHN W.
<u>11040845</u>	Not Issued	41	01/21/2005	Communication system with low power, DC-balanced serial link	POULTON, JOHN W.
<u>11057078</u>	7078979	150	02/11/2005	PHASE CONTROLLED OSCILLATOR CIRCUIT WITH INPUT SIGNAL COUPLER	POULTON, JOHN W.
<u>11107121</u>	Not Issued	20	04/15/2005	Processor controlled interface	POULTON, JOHN W.
<u>11217109</u>	Not Issued	71	08/30/2005	Combined phase comparator and charge pump circuit	POULTON, JOHN W.
<u>11336045</u>	Not Issued	25	01/20/2006	High-speed signaling systems with adaptable pre-emphasis and equalization	POULTON, JOHN W.
<u>11342780</u>	Not Issued	30	01/30/2006	Low power, DC-balanced serial link transmitter	POULTON, JOHN W.
<u>11407371</u>	Not Issued	30	04/18/2006	Signaling system with low-power automatic gain control	POULTON, JOHN W.
<u>11440824</u>	Not Issued	20	05/25/2006	Phase controlled oscillator circuit with input signal coupler	POULTON, JOHN W.
<u>60181276</u>	Not Issued	159	02/09/2000	Transition-time control for a high-speed data transmitter	POULTON, JOHN W.
<u>60269984</u>	Not Issued	159	02/20/2001	Clock multiplier interpolation and filtering	POULTON, JOHN W.
<u>60572508</u>	Not Issued	159	05/18/2004	Multi-phase and multi-rate clock generation	POULTON, JOHN W.
<u>60645823</u>	Not Issued	159	01/20/2005	High-speed signaling systems with adaptable pre-emphasis and equalization	POULTON, JOHN W.
<u>06408045</u>	4783649	150	08/13/1982	VLSI GRAPHICS DISPLAY IMAGE BUFFER USING LOGIC ENHANCED PIXEL MEMORY CELLS	POULTON, JOHN W.
<u>07975821</u>	5388206	250	11/13/1992	ARCHITECTURE AND APPARATUS FOR IMAGE GENERATION	POULTON, JOHN W.
<u>08383969</u>	5481669	250	02/06/1995	ARCHITECTURE AND APPARATUS FOR IMAGE GENERATION UTILIZING	POULTON, JOHN W.

				ENHANCED MEMORY DEVICES	
09302461	6556628	150	04/29/1999	METHODS AND SYSTEMS FOR TRANSMITTING AND RECEIVING DIFFERENTIAL SIGNALS OVER A PLURALITY OF CONDUCTORS	POULTON, JOHN W.
09414761	6275072	150	10/07/1999	COMBINED PHASE COMPARATOR AND CHARGE PUMP CIRCUIT	POULTON, JOHN W.
09453368	6316987	150	12/01/1999	LOW-POWER LOW-JITTER VARIABLE DELAY TIMING CIRCUIT	POULTON, JOHN W.
11070154	Not Issued	25	03/01/2005	Electrostatic discharge protection for a fingerprint sensor	POULTON, JOHN WOOD
11227625	Not Issued	20	09/15/2005	Power supply shunt	POULTON, JOHN WOOD

Inventor Search Completed: No Records to Display.

Search Another: Inventor	Last Name	First Name	<input type="button" value="Search"/>
	<input type="text" value="POULTON"/>	<input type="text" value="JOHN"/>	

To go back use Back button on your browser toolbar.

Back to [PALM](#) | [ASSIGNMENT](#) | [OASIS](#) | [Home page](#)